# **Department of Computer Science and Engineering**

### **BRAC University**

### **CSE 260: Digital Logic Design**

# **Experiment # 7**

***Design a circuit that outputs 2’s complement of a 3 bit number using encoder & decoder.***

***IC: 74ls138 [decoder]; 74ls148 [encoder]***

*The Truth Table for 2’s complement output:*

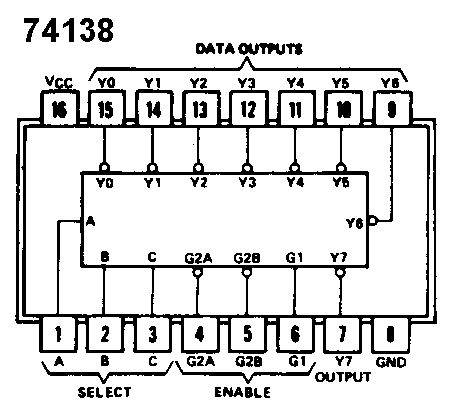
| Inputs | | | | Outputs | | | | Active Low Output | | | Output line Connection | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Minterm | C | B | A | Minterm | D2 | D1 | D0 | D2 | D1 | D0 | Decoder | Encoder |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 7 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 7 |
| 2 | 0 | 1 | 0 | 6 | 1 | 1 | 0 | 0 | 0 | 1 | 2 | 6 |
| 3 | 0 | 1 | 1 | 5 | 1 | 0 | 1 | 0 | 1 | 0 | 3 | 5 |
| 4 | 1 | 0 | 0 | 4 | 1 | 0 | 0 | 0 | 1 | 1 | 4 | 4 |
| 5 | 1 | 0 | 1 | 3 | 0 | 1 | 1 | 1 | 0 | 0 | 5 | 3 |
| 6 | 1 | 1 | 0 | 2 | 0 | 1 | 0 | 1 | 0 | 1 | 6 | 2 |
| 7 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 7 | 1 |

**Report:**

The report should cover the followings

1. Name of the experiment
2. Objective
3. Required Components and Equipments
4. Experimental Setup (i.e., diagram of the circuit)
5. Results and Discussions
   1. Draw a circuit diagram with encoder and decoder that will output the 1’s complement of 3 bit number.
   2. Can you implement a code converter with encoder and decoder? If yes, how? If no, explain why not?





**74148**

